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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,326	12/21/2001	Lee D. Whetsel	TI-32417	4256

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/028,326	Applicant(s) WHETSEL, LEE D.	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 are pending and are presented for examination.

Specification

2. The abstract of the disclosure is objected to because it lacks proper language and format for an abstract.

On line 1, the phrase "This disclosure describes" should be deleted. Also, the phrase, "An IEEE P1500 standard is in development" and any other term related to "P1500" should be removed from the abstract because the P1500 is still in development and therefore it is beyond the scope of the claimed invention, since there is not enough information available to a person of ordinary skill in the art to make or use the invention. Applicant is reminded of the proper language and format for an abstract of the disclosure. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Pressly et al. (US 5889788), issued: March 30, 1999.

Regarding independent Claim 1, Pressly discloses an apparatus for wrapper cell test architecture within an integrated circuit (10, FIG. 1), comprising:

A plurality of core wrappers (16 and 18) each free of 1149.1 test access ports, each having a serial input, a serial output, and control inputs, such as a test ring select enable (TRSE) and a test enable (TRTE1) signal, (FIG. 1, also, see abstract). Pressly discloses core wrapper testing without the implementation of IEEE 1149.1 boundary scan architecture, since the scan test architecture does not interface with TAP controller and JTAG test system. For the purpose examination, it is noted that a "wrapper" surrounding the embedded core 14 contains many cells similar to 16 and 18. However, only two cells 16 and 18 are illustrated in FIG. 1 by way of example.

Input circuitry, which is part of the input section of logic (12) having control inputs, serial input (INPUT), and a plurality of serial outputs though core wrapper (16), which provide scan data outputs (SDO1) and (SDO2) to core 14 (col. 6, lines 60-65).

Output circuitry, which is part of the output section of logic (12), having control inputs, a plurality of serial inputs, and a serial output (OUTPUT) through core wrapper (16) corresponding to scan data input (SDI1) and (SDI2) from core 14. Logic 12 can be an input port, an output port, a peripheral interface or any logic circuitry, which can be integrated on the same substrate material with the embedded core to form a complete microcontroller, (col.6, lines 47-50).

First connections formed between the serial outputs from the input section of logic 12 and the serial inputs of the plurality of core wrappers (16).

Second connections formed between the serial outputs from the plurality of core wrappers (18) and the serial inputs coupled to the output section of logic (12).

Regarding Claim 9, Pressly discloses an apparatus for wrapper cell test architecture within an integrated circuit (10, FIG. 1), comprising:

A plurality of circuits, such as input and output section of logic (12), each having an input and an output, FIG. 1.

A data path formed between the output of the input section of logic (12) and core wrapper (16) corresponding to (SDO1) serial data out path, and between the input of the output section of logic (12) and core wrapper (18) corresponding to (SDI1) serial data in path, FIG. 1.

Circuitry (MUX) 24 within the (SDO1) serial data out path of core wrapper (16) selectively operating in a normal mode "0" for providing a normal mode data path between logic 12 and the embedded core 14 and selectively operating in a test mode by setting (TRTE1) signal "1", thereby selecting test data. Also, (MUX) 30 (SDI1) within serial data in path of core wrapper (18) operate the same as (MUX) 24, for providing normal or test data from the output of the embedded core 14.

Regarding Claim 2, Pressly discloses third connections between the control inputs of test ring select enable (TRSE) and test enable (TRTE1) signal of the core wrappers (16 and 18), (FIG. 1, also, see abstract).

Regarding Claim 3, Pressly discloses a plurality of test architectures connected in a serial arrangement and containing many cells similar to (16 and 18), which is arranged in parallel between input circuitry (input section of logic, 12) and output

circuitry (output section of logic 12). The serial inputs to the input circuitry of the plurality of test architectures (16) are connected to outputs from the input circuitry and the serial outputs from the output circuitry of the plurality of test architectures (18) are connected to inputs to the output circuitry.

Regarding Claims 4 and 5, Pressly discloses a plurality of test architectures connected in a serial arrangement containing many cells similar to (16 and 18). The serial output of the output circuitry of one test architecture (16) is connected to serial input of the input circuitry of another test architecture (18) through a circuit, such as embedded core 14, FIG. 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pressly et al. (US 5889788).

Regarding independent Claims 6, 7 and 8, Pressly discloses the common limitations recited in claim 1. Pressly does not disclose a shift register having an input connected to the output of the output circuitry, external to the wrapper arrangement.

However, Pressly discloses logic 12 having external signals designated as (INPUTS) and (OUTPUTS) terminals which can interface with an external microcontroller. Logic 12 is a customer specified logic circuitry, which can be a memory array, an input or an output port, a peripheral interface or any logic circuitry for interfacing with the microcontroller. Logic 12 performs most of the communication with the external terminals of the integrated circuit 10 via the inputs and outputs illustrated in FIG. 1. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to shift serial data from the core wrapper (18) to the external microcontroller, as taught by Pressly, through the external serial data output terminal, since a shift register is normally part of microcontroller, thus avoiding the need for an additional register.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 29 April 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100